Front end electronics for TPC

Takao

BNL

Design parameters

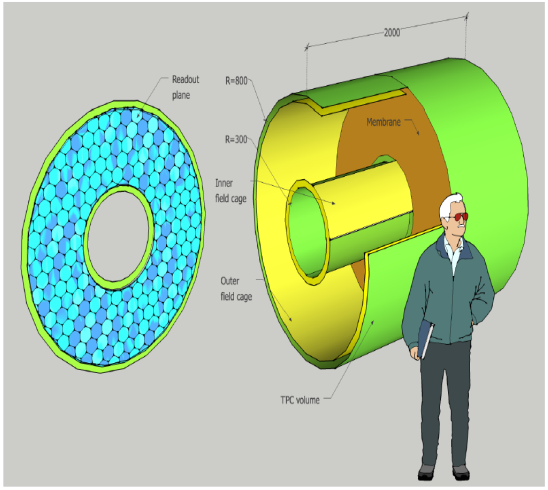
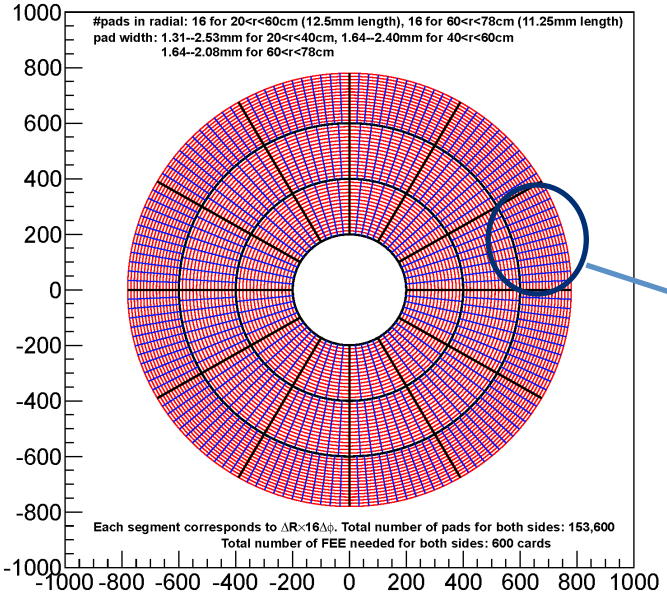
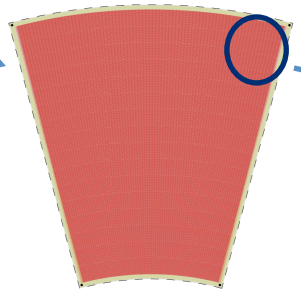
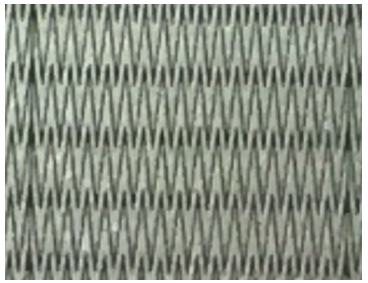


Figure 4.26: Schematic layout of TPC main elements.

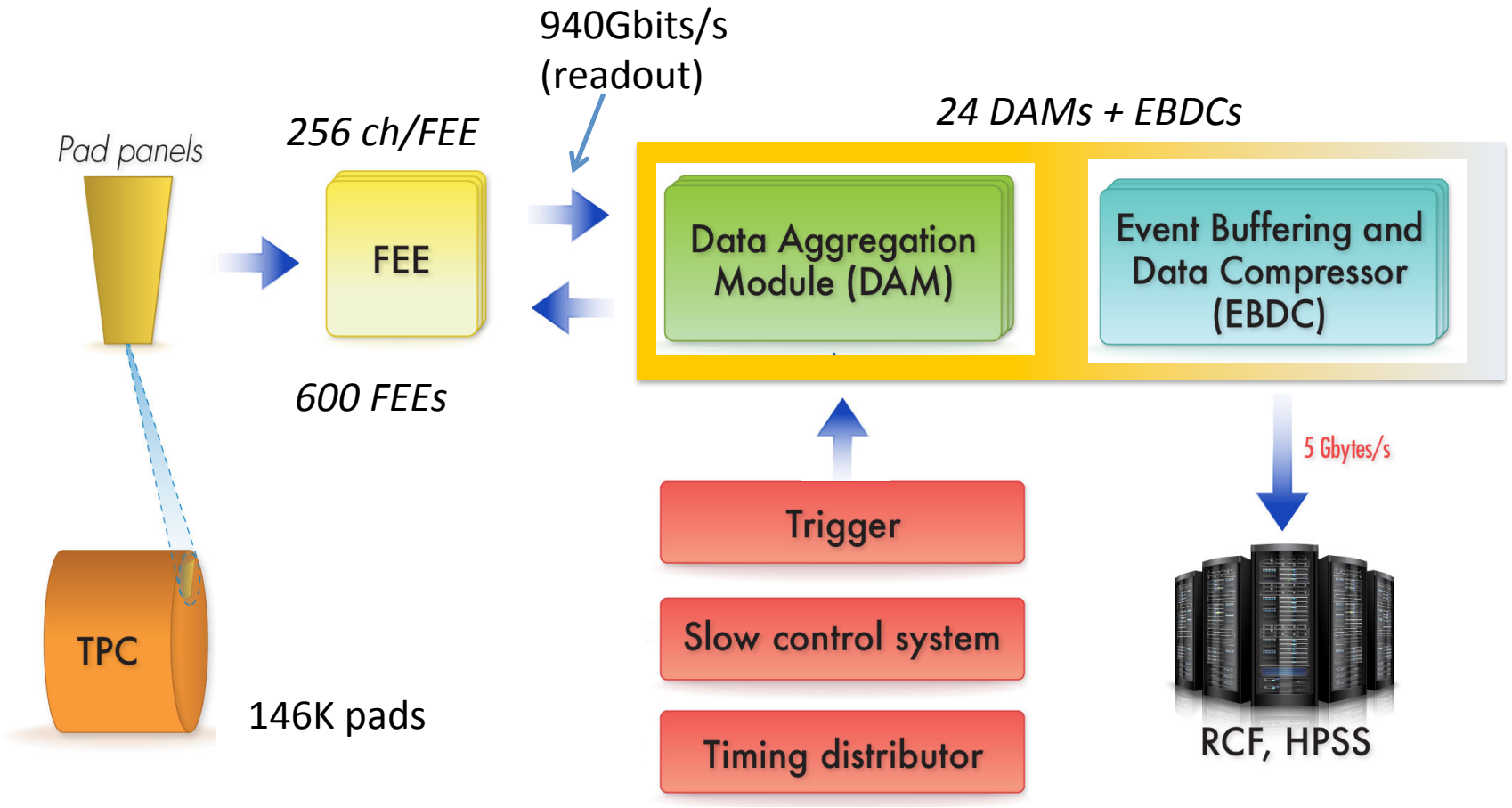






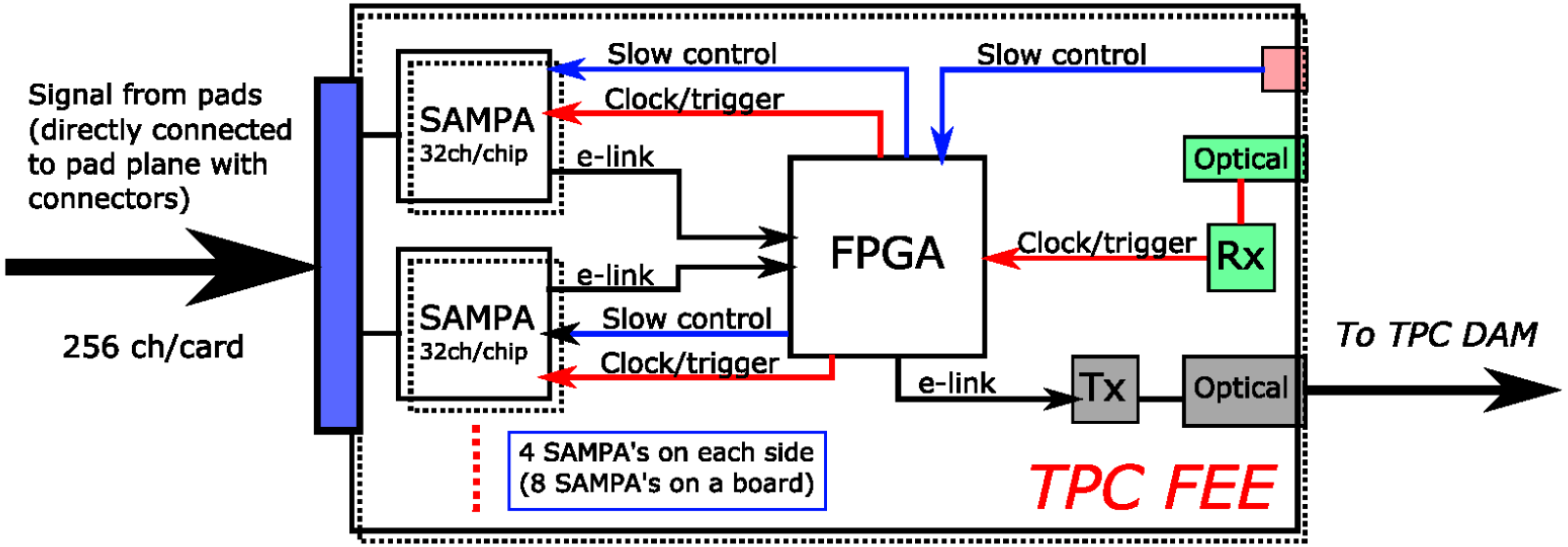
- 146K readout channels from both ends
  - 40 measurements (clusters) in radial direction
- 15KHz is the baseline trigger rate
  - limit of DAQ rate prior to livetime fall-off
  - We assume that beam interaction may happen as much as 100KHz for $|z|<1$m
- $dN_{ch}/dy = 180$ (minbias Au+Au @ 200GeV) → 400 tracks in $|\eta|<1.1$
  - Background and fakes effectively doubles the number of tracks; 800 tracks in the TPC
- Raw rate: 940Gbits/s @ 100KHz
  - Caveat: Radially-averaged rate
  - η dependent acceptance change is taken into account

Overall scheme (Apr 1, 2017)



FEE (Frontend)

- Each FEE takes care of 256 inputs. 146K ch ~ 600 FEEs
  - Use of SAMPA chips (SAMPA is “shaper + ADC + DSP”)
  - SAMPA accepts 32 inputs → 8 SAMPAs on a board (4 SAMPAs on each side)
- FPGA receives and distributes slow control and timing/clock signal
- FPGA also collects digitized data from SAMPAs (e-link) and send them out to DAM module via optical transmission
  - We don’t need to use GBT protocol



We rely on SAMPA

- SAMPA = CSA + Shaper + ADC + DSP
  - 32 channels input
  - Maximum e-link output: 28Gbits/sec per chip. 11 e-link lines available
- Prototype chip is available now. Next version of SAMPA will be pre-final
  - Current SAMPA has reference voltage and some DSP issues

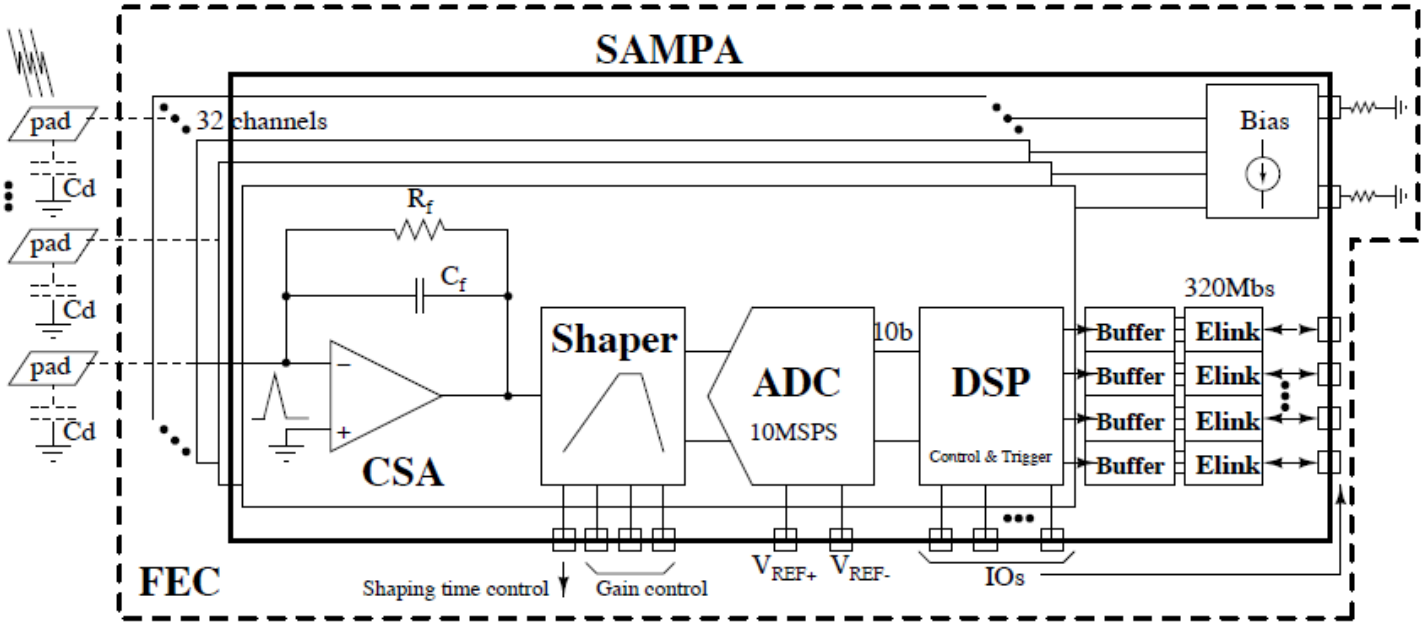
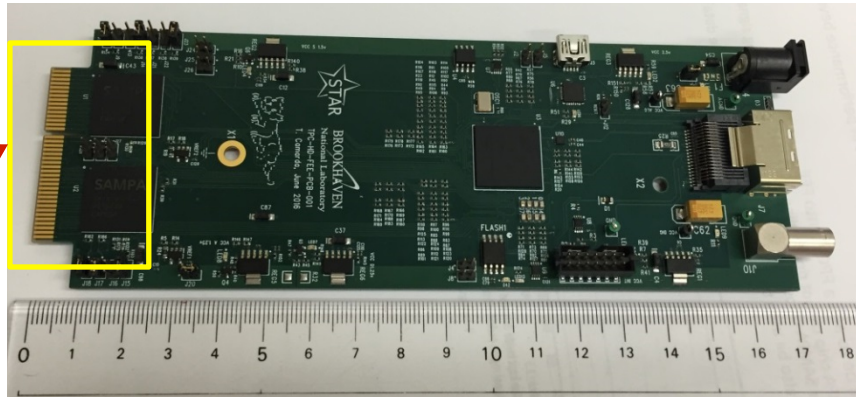


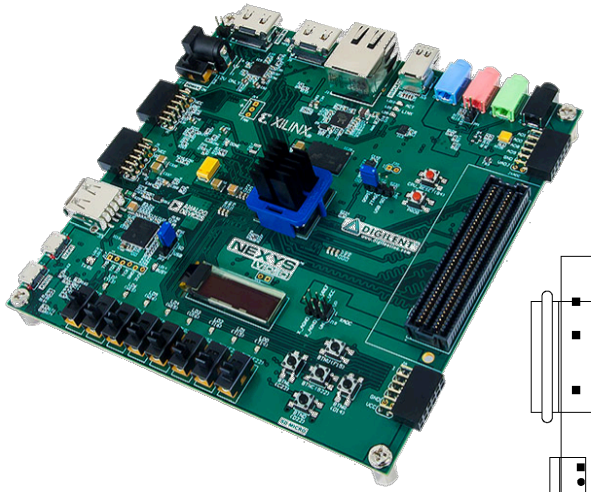
Figure 6.4: Schematic of the SAMPA ASIC for the GEM TPC readout, showing the main building blocks.

Development status

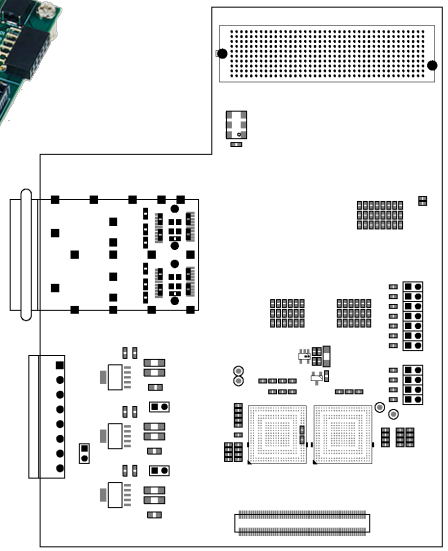
- STAR iFEE is provided by the courtesy of Tonko Ljubicic
- Geometry of the card is 62mm*62mm
  - 64 channels/card (32 ch/SAMPA)
  - One SAMPA chip is 15*15mm^2
  - SAMPA is working as expected



- Design of pre-prototype FEE board is done
  - Board consists of two SAMPAs and a SPF
  - Purpose it check interface of SAMPA and FPGA
  - FPGA is from Artix-7 evaluation board

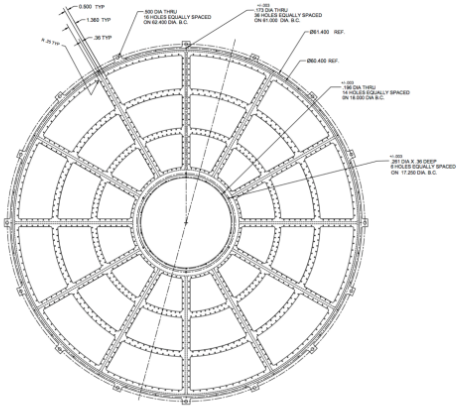


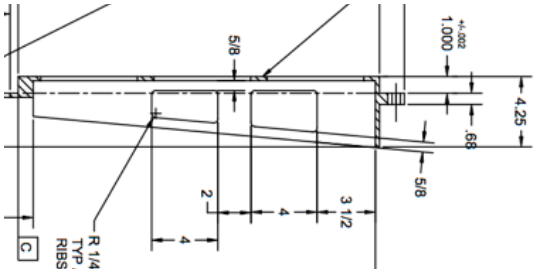
- Connector of the pre-prototype board matches the one on the prototype padplane that Bob Azmon et al. designed
  - Signal from padplane will be an input to the pre-prototype board
  - Check cross-talk on the padplane, etc.

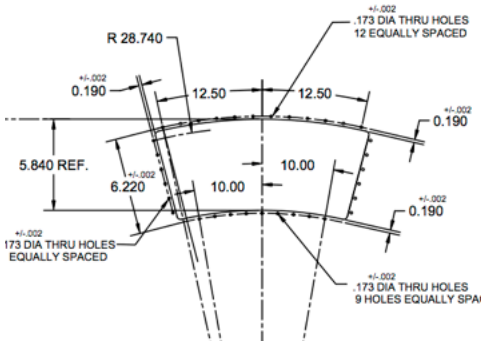


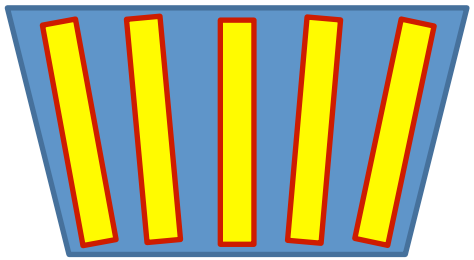
Placing FEE at the endcap

- From the previous pad layout, the minimum spacing of the FEE cards will be ~2cm (at r=20cm)
  - This is acceptable from the point of view of engineering
- It fits to the support structure at the endcap
  - Board width should be <14.8cm
  - Board length should be <10cm
  - Board spacing should be <2cm

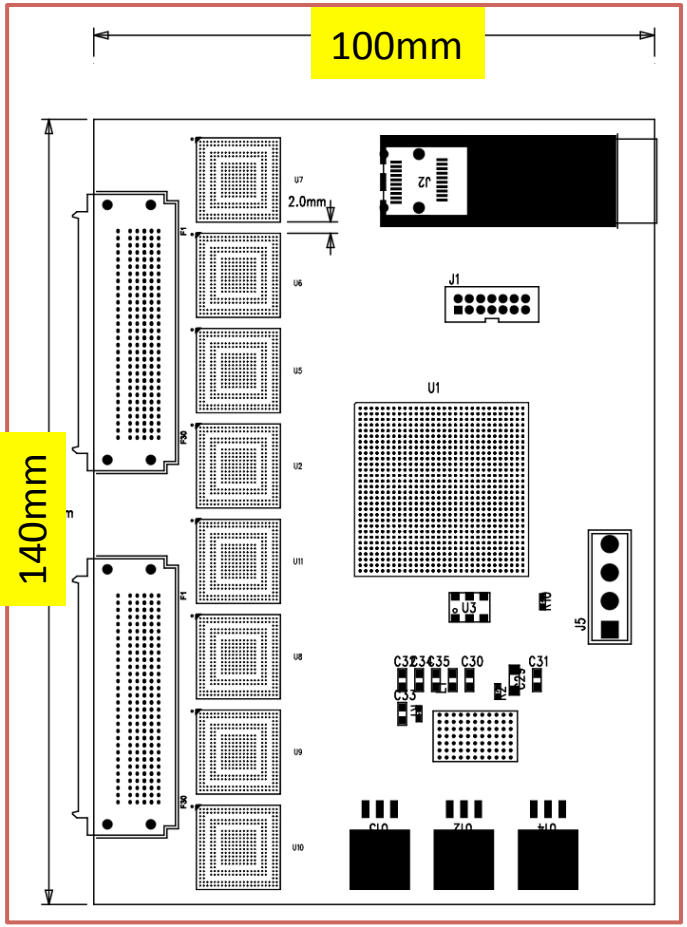




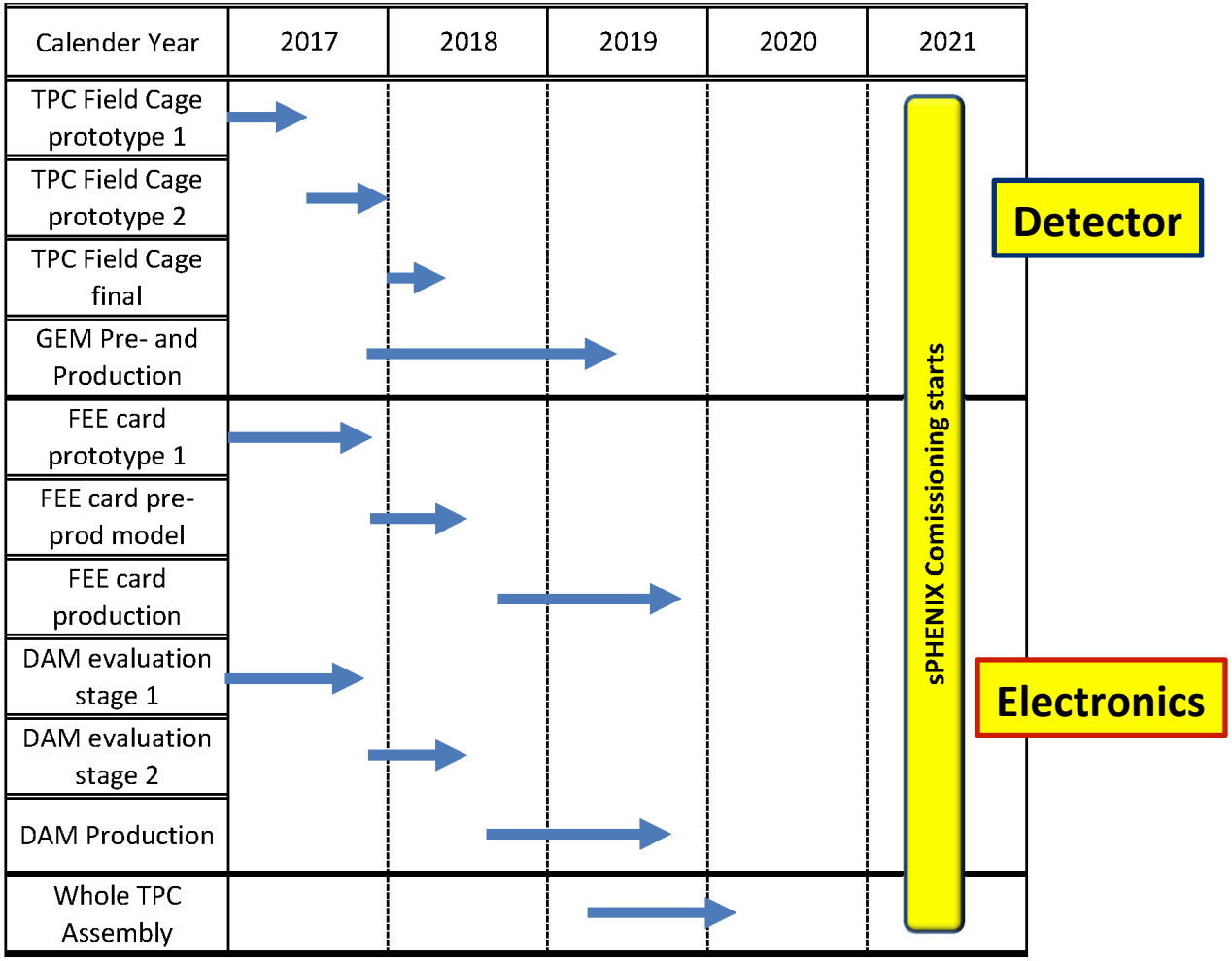




Full-scale Prototype v1



Schedule


Calender Year
2017
2018
2019
2020
2021
TPC Field Cage prototype 1
TPC Field Cage prototype 2
TPC Field Cage final
GEM Pre- and Production
FEE card prototype 1
FEE card pre-prod model
FEE card production
DAM evaluation stage 1
DAM evaluation stage 2
DAM Production
Whole TPC Assembly
sPHENIX Comissioning starts
Detector
Electronics

Costs review for FEE (prototype)

- Total: $60K for v1, and $30K for pre-production

1.2.6.1	TPC FEE Prototype v1						$57,330
1.2.6.1.3	Procure TPC FEE prototype v1 components					$16,500	
		SAMPA chip	CERN	$9,000	200 chips (~$45/chip from Tonko's info) for 25		
		FPGA (Artix-7)	Xilinx	$2,500	Joe's experience (25 boards)		
		Optical transmitter/receiver	Avago	$1,250	Joe's experience (25 boards)		
		Resistor/capacitor/regulator	Digikey	$2,500	Joe's experience (25 boards)		
		Card Connectors	Samtec	$1,250	Joe's experience (25 boards)		
1.2.6.1.4	Fabricate TPC FEE prototype v1 boards					$7,500	
		Initial fee		$5,000	Joe's experience		
		Board fabrication		$2,500	Joe's experience (25 boards)		
1.2.6.1.5	Procure TPC FEE prototype v1 LV power supplies					$5,100	
		MegaPac Chassis (5V)	Vicor West Coast	$5,100	Steve's Quote (Jan, 2016), 1 module		
1.2.6.1.6	Develop TPC FEE Test Stand					$26,980	
		Chain test board fabrication	BNL	$2,000			
		Resistor/capacitor/regulator	Digikey	$100			
		Optical transmitter/receiver	Avago	$50			
		SAMPA chip	CERN	$180	Two chips (with spare of 2)		
		FPGA (Artix-7)	Xilinx	$100	Manufacturer Quote		
		Card Connectors	Samtec	$50			
		Pulse distributor board initial fee	BNL	$2,000			
		Pulse distributor	BNL	$7,500	guess (25 input selectors)		

Costs review for FEE (mass prod.)

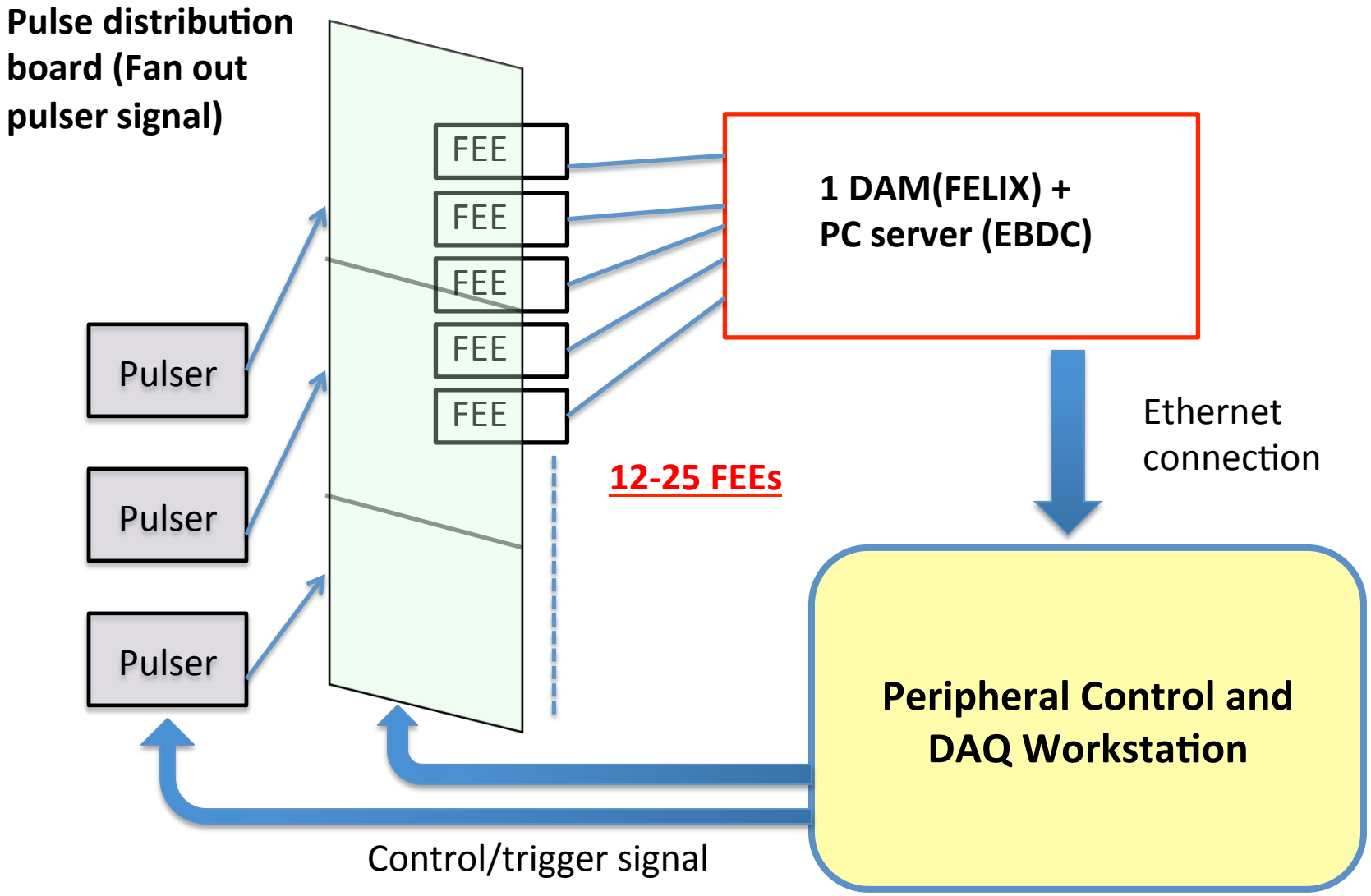
- Total: $800K (with power supply and cable), including 25% spare

1.2.6.3	TPC FEE Production						$782,600
1.2.6.3.1	Procure TPC FEE components					$603,000	
		SAMPA chip	CERN	$378,000	4800 + 3600 chips (~$45/chip)		
		FPGA (Artix-7)	Xilinx	$75,000	100 * 600 +25% spare		
		Optical transmitter/receiver	Avago	$37,500	50 * 600 + 25% spare		
		Resistor/capacitor/regulator	Digikey	$75,000	100 * 600 + 25% spare		
		Card Connectors	Samtec	$37,500	50 * 600 + 25% spare		
1.2.6.3.2	Procure TPC FEE LV power supplies					$62,100	
		10AWG 6T00UP Cable	Belden	$6,000	$1.5/ft, 4000ft.		
		MegaPac chassis (5V)	Vicor West Coast	$56,100	5100 * 10 + 1 spare		
1.2.6.3.3	Fabricate and assemble all TPC Fee boards					$117,500	
		Initial fee		$5,000			
		Board fabrication		$75,000	100 * 600 + 25% spare		
		Parts mounting		$37,500	50 * 600 + 25% spare		

Radiation

- Initial radiation estimate is estimated
  - Eric's analysis result of RadFET monitoring during Run-14 Au+Au 200GeV run
  - Delivered luminosity to PHENIX was 23 nb^{-1}
- Measured result
  - 100Gy at r=3.5cm, 50Gy at r=6.5cm, 15Gy at r=16cm
  - Simple $1/r^2$ dependence
- Total Dose at TPC (@100KHz): 10μGy/sec at 16cm
  - Highest radiation possible at TPC
- Neutron flux (1 MeV Equivalent Fluence):
  - 1.1×10^{10} n/cm^2 at r=16cm, 1.5×10^{10} n/cm^2 at 3.5cm and 6.5cm
  - ~1.0×10^{4} n/cm^2/sec at 16cm (@ 100KHz)

Test stand scheme



Final words

- Development of the TPC FEE is in flow
- Pre-prototype will be produced soon
- Prototype v1 will also be produced in a couple of months

Support Materials

Schedules and funding news

- All the development should be finished by Jul 2018
  - Pre-prototype, prototype v1 and pre-production prototype

- Use of OPC fund is just approved
  - Enough funding for all the prototype development
  - $90K for FEE, $40K for DAM/EBDC

sPHENIX PROJECT SCHEDULE (Modified to fit updated DOE/CD Milestones)

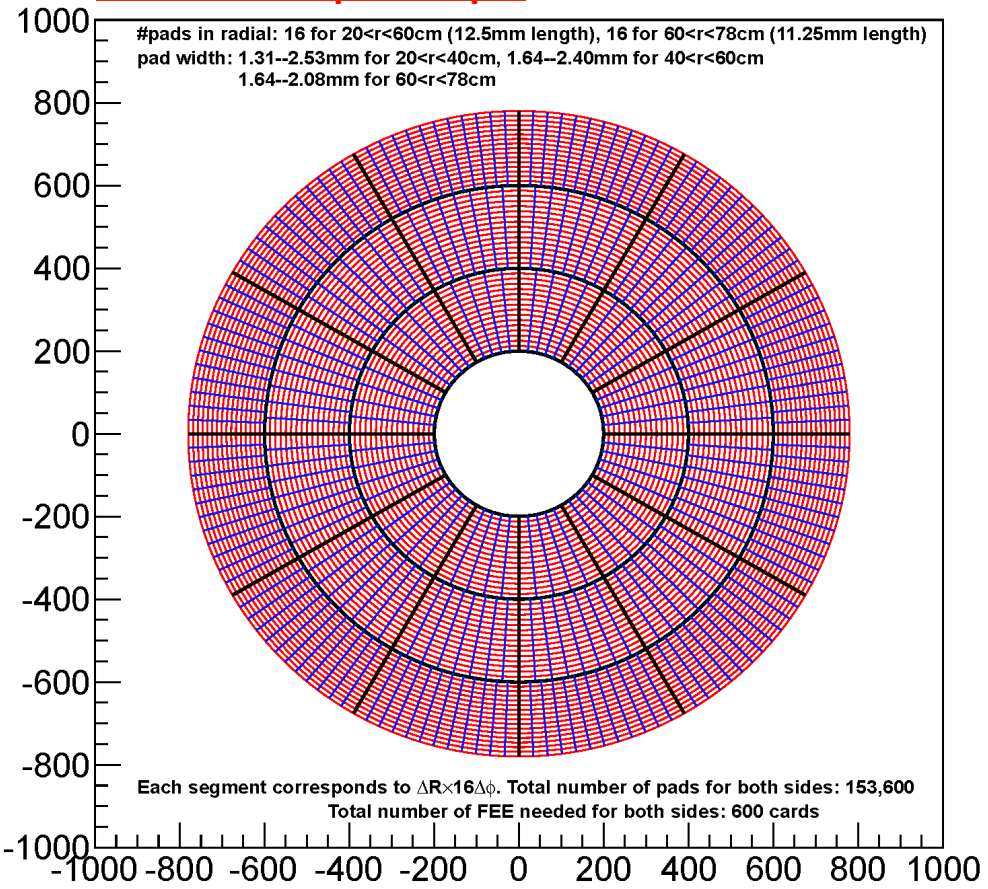
WBS	Task Name	Duration	Start	Finish	Predecessors	Successors	Resource Names	Fixed Cost
1.2.6	**TPC FEE**	**696 days**	**Thu 9/22/16**	**Wed 7/10/19**				**$0**
1.2.6.1	**TPC FEE Prototype v1**	**230 days**	**Thu 9/22/16**	**Wed 8/23/17**				**$0**
1.2.6.1.1	Write TPC FEE prototype v1 design specification	10 days	Thu 9/22/16	Wed 10/5/16	2	183	SCI3 PO[30%],PROF4 PO E[35%],TECH3 PO D[35%]	$0
1.2.6.1.2	Design TPC FEE protoype v1	135 days	Thu 10/6/16	Fri 4/21/17	182	184,186,187	PROF4 PO E[50%],TECH3 PO D[50%]	$0
1.2.6.1.3	Procure TPC FEE prototype v1 components	15 days	Mon 4/24/17	Fri 5/12/17	183	185	PROF4 PO E[10%]	$11,000
1.2.6.1.4	Fabricate TPC FEE prototype v1 boards	30 days	Mon 5/15/17	Mon 6/26/17	184	188	PROF4 PO E[10%]	$8,000
1.2.6.1.5	Procure TPC FEE prototype v1 LV power supplies	5 days	Mon 4/24/17	Fri 4/28/17	183	188	SCI3 PO[10%],PROF4 PO E[10%],TECH3 PO D[10%]	$12,000
1.2.6.1.6	Develop TPC FEE Test Stand	40 days	Mon 4/24/17	Mon 6/19/17	183	188	SCI3 PO[10%],PROF4 PO E[25%],TECH3 PO D[30%],TECH3 PO E[	$150,000
1.2.6.1.7	Assemble and test TPC FEE prototype v1	40 days	Tue 6/27/17	Wed 8/23/17	187,186,185	190	SCI3 PO[10%],PROF4 PO E[20%],TECH3 PO D[20%],TECH3 PO E[	$2,000
1.2.6.2	**TPC FEE Pre-Production**	**155 days**	**Thu 8/24/17**	**Tue 4/10/18**				**$0**
1.2.6.2.1	Design TPC FEE preproduction protoype	70 days	Thu 8/24/17	Tue 12/5/17	188	191,193	PROF4 PO E[50%],TECH3 PO D[50%]	$0
1.2.6.2.2	Procure TPC FEE preproducion prototype compor	15 days	Wed 12/6/17	Thu 12/28/17	190,4	192	PROF4 PO E[10%]	$11,000
1.2.6.2.3	Fabricate TPC FEE preproduction prototype boar	30 days	Fri 12/29/17	Mon 2/12/18	191	194	PROF4 PO E[10%]	$8,000
1.2.6.2.4	Modify TPC FEE Test Stand	30 days	Wed 12/6/17	Mon 1/22/18	190	194	SCI3 PO[10%],PROF4 PO M[25%],TECH3 PO D[30%],TECH3 PO E[	$8,000
1.2.6.2.5	Assemble and test TPC FEE preproduction protot	40 days	Tue 2/13/18	Tue 4/10/18	193,192	196	SCI3 PO[10%],PROF4 PO E[20%],TECH3 PO D[20%],TECH3 PO E[	$2,000
1.2.6.3	**TPC FEE Production**	**212 days**	**Fri 8/31/18**	**Wed 7/10/19**				**$0**
1.2.6.3.1	Procure TPC FEE components	70 days	Fri 8/31/18	Thu 1/31/19	6,194	198	SCI3 Other[10%],PROF4 PO E[50%],TECH3 PO D[40%]	$221,000
1.2.6.3.2	Procure TPC FEE LV power supplies	40 days	Fri 8/31/18	Fri 10/26/18	6		PROF4 PO E[10%]	$84,000
1.2.6.3.3	Fabricate and assemble all TPC Fee boards	55 days	Fri 2/1/19	Fri 4/19/19	196	200	PROF4 PO E[10%]	$200,000
1.2.6.3.4	Procure TPC FEE Optical Fibers	40 days	Fri 8/31/18	Fri 10/26/18	6	200	PROF4 PO E[10%]	$100,000
1.2.6.3.5	Perform QA Testing on TPC FEE	55 days	Mon 4/22/19	Wed 7/10/19	198,199	118	SCI3 Other[10%],PROF4 PO E[10%],TECH3 Other[30%],STUDENT	$0
1.2.7	**TPC DAM**	**734 days**	**Thu 9/22/16**	**Tue 9/3/19**				**$0**
1.2.7.1	**TPC DAM Evaluation --FELIX 1.5**	**180 days**	**Thu 9/22/16**	**Mon 6/12/17**				**$0**
1.2.7.1.1	Write Design Spec for TPC DAM prototype v1	110 days	Thu 9/22/16	Fri 3/3/17	2	204	SCI3 PO[30%],PROF4 PO E[35%],TECH3 PO D[35%]	$0
1.2.7.1.2	Develop TPC DAM prototype v1 Test Stand	40 days	Mon 3/6/17	Fri 4/28/17	203	205	PROF4 PO E[50%],TECH3 PO D[50%]	$12,000
1.2.7.1.3	Measure TPC DAM prototype v1 Throughput	30 days	Mon 5/1/17	Mon 6/12/17	204		PROF4 PO E[50%],TECH3 PO D[50%]	$0
1.2.7.2	**TPC DAM Evaluation -- FELIX 2.0**	**105 days**	**Mon 12/4/17**	**Fri 5/4/18**				**$0**
1.2.7.2.1	Procure FELIX 2.0 board for TPC DAM	15 days	Mon 12/4/17	Tue 12/26/17	4	208	PROF4 PO E[10%]	$12,000
1.2.7.2.2	Measure Throughput of FELIX 2.0 for TPC DAM	30 days	Wed 12/27/17	Thu 2/8/18	207	209	PROF4 PO E[10%]	$0
1.2.7.2.3	Develop TPC DAM FPGA Algorithm	60 days	Fri 2/9/18	Fri 5/4/18	208		SCI3 Other[10%],PROF4 PO E[25%],TECH3 PO D[30%],TECH3 PC	$0
1.2.7.3	**TPC DAM Production**	**250 days**	**Fri 8/31/18**	**Tue 9/3/19**				**$0**
1.2.7.3.1	Procure TPC DAM Felix 2.0 boards	75 days	Fri 8/31/18	Wed 12/19/18	6	212	SCI3 Other[10%],PROF4 PO E[50%],TECH3 PO D[40%]	$300,000
1.2.7.3.2	Perform QA Testing on TPC DAM FELIX 2.0 boards	55 days	Thu 12/20/18	Wed 3/13/19	211	214	SCI3 Other[10%],PROF4 PO E[10%],TECH3 PO E[30%],STUDENT[	$0
1.2.7.3.3	Procure of TPC EDBC Computers and Peripherals	60 days	Fri 8/31/18	Mon 11/26/18	6	214	SCI3 Other[30%],PROF4 PO E[40%],TECH3 PO D[30%]	$150,000
1.2.7.3.4	Test Full TPC DAM System	120 days	Thu 3/14/19	Tue 9/3/19	213,212		SCI3 Other[50%],PROF4 PO E[50%]	$0

Pad side update

- New pad layout (20<r<78cm)
  - Three segments in radial direction, each divided into 16
  - 12 segments in phi direction, each divided into multiple of 16
  - Matching to number of input to a FEE
  - Each cell in the right figure corresponds to 16 pads in phi
- Variable pad size as a function of radial position
- Total 153,600 pads for both side
  - 600 FEE cards
- Data Rate (no header included)
  - 1.42Gbps/board for 30<r<40cm
  - 1.45Gbps/board for 40<r<60cm
  - 0.77Gbps/board for 60<r<80cm
  - → 28Gbps/(1/12 full azimuth)

5 FEEs for 20<r<40cm, 8 for 40<r<60cm, 12 for 60<r<78cm, for each 1/12 of full azimuth

Each cell = 16pads in phi



Alternate option? CRU ≅ DAM+EBDC

- ALICE is developing a CRU, which bases on the similar card developed by LHCb
- CRU interfaces the FEC and online computer farm
- All of slow control and timing distribution, and data transmission are realized by optical connection.
  - According to John Haggerty, this was an option for the PHENIX readout system?

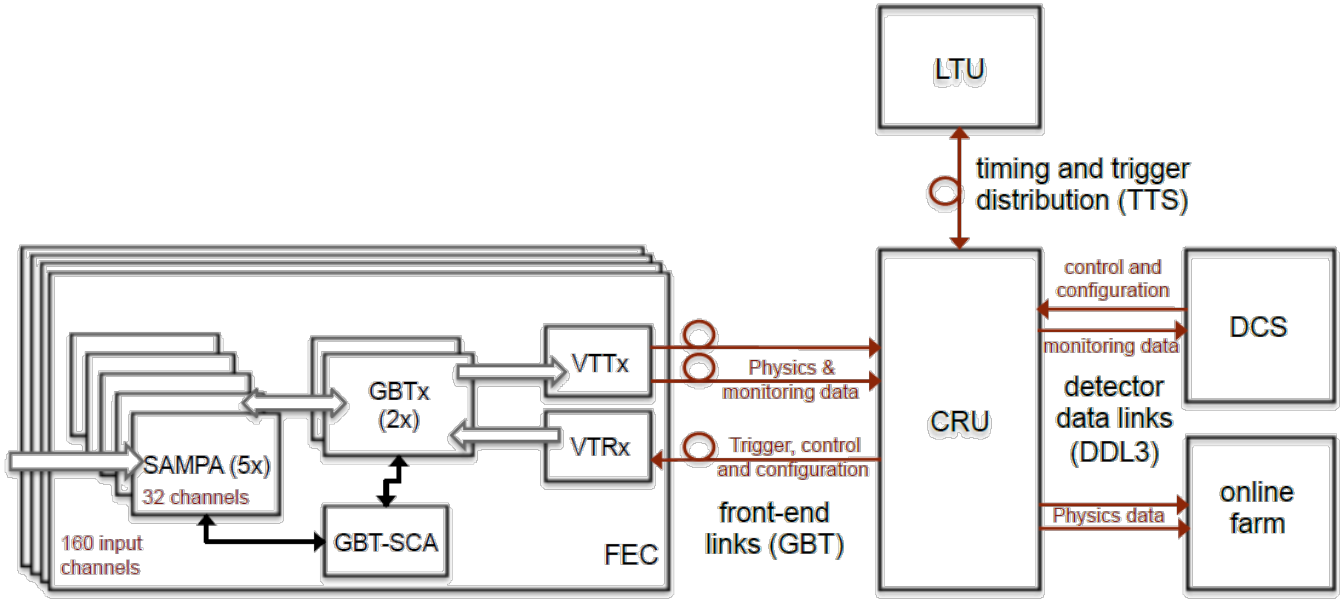


Figure 6.9: Schematic of the TPC readout system with the CRU as central part interfacing the front-end electronics to the trigger system, the DCS and the online farm.

Data rate (two cases)

- Data Rate with zero-suppression
  - 1.42Gbps/board for 30<r<40cm
  - 1.45Gbps/board for 40<r<60cm
  - 0.77Gbps/board for 60<r<80cm
  - → 28Gbps/(1/12 full azimuth)

- With no zero-suppression in SAMPA (common-mode noise case)
  - 26Gbps/board (fixed)
    - No way to send this amount of data through one optical link?
  - FPGA on FEE has to do job
    - Need to take care of 11*8 e-links from 8 SAMPAs
    - Average out the charges in pads that have negative values (> 50 pads?)
    - Shift other channels by that amount

- No header is included in the estimate above
  - 40% increase (max) of the data volume for zero-suppression mode
  - Less than 1% increase for non zero-suppression mode

Costs review for FEE (prototype)

- Total: $60K for v1, and $30K for pre-production

1.2.6.1	TPC FEE Prototype v1						$57,330
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		FPGA (Artix-7)	Xilinx	$2,500	Joe's experience (25 boards)		
		Optical transmitter/receiver	Avago	$1,250	Joe's experience (25 boards)		
		Resistor/capacitor/regulator	Digikey	$2,500	Joe's experience (25 boards)		
		Card Connectors	Samtec	$1,250	Joe's experience (25 boards)		
1.2.6.1.4	Fabricate TPC FEE prototype v1 boards					$7,500	
		Initial fee		$5,000	Joe's experience		
		Board fabrication		$2,500	Joe's experience (25 boards)		
1.2.6.1.5	Procure TPC FEE prototype v1 LV power supplies					$5,100	
		MegaPac Chassis (5V)	Vicor West Coast	$5,100	Steve's Quote (Jan, 2016), 1 module		
1.2.6.1.6	Develop TPC FEE Test Stand					$26,980	
		Chain test board fabrication	BNL	$2,000			
		Resistor/capacitor/regulator	Digikey	$100			
		Optical transmitter/receiver	Avago	$50			
		SAMPA chip	CERN	$180	Two chips (with spare of 2)		
		FPGA (Artix-7)	Xilinx	$100	Manufacturer Quote		
		Card Connectors	Samtec	$50			
		Pulse distributor board initial fee	BNL	$2,000			
		Pulse distributor	BNL	$7,500	guess (25 input selectors)		

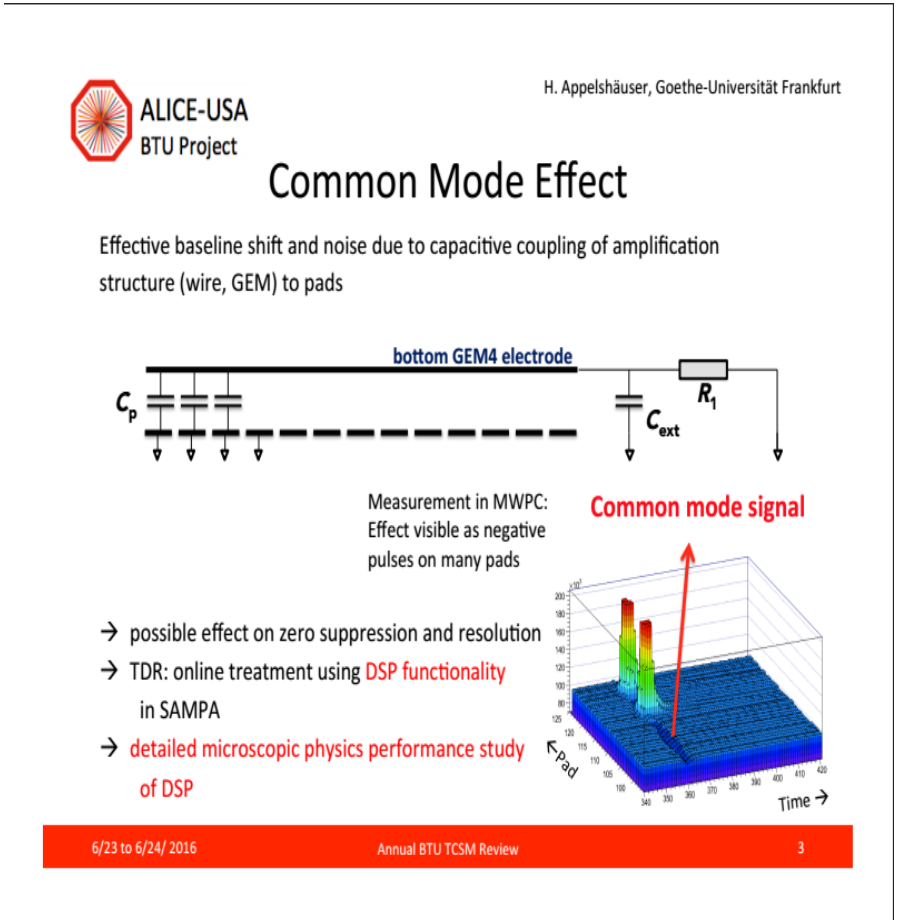
Costs review for FEE (mass prod.)

- Total: $800K (with power supply and cable), including 25% spare

1.2.6.3	TPC FEE Production						$782,600
1.2.6.3.1	Procure TPC FEE components					$603,000	
		SAMPA chip	CERN	$378,000	4800 + 3600 chips (~$45/chip)		
		FPGA (Artix-7)	Xilinx	$75,000	100 * 600 +25% spare		
		Optical transmitter/receiver	Avago	$37,500	50 * 600 + 25% spare		
		Resistor/capacitor/regulator	Digikey	$75,000	100 * 600 + 25% spare		
		Card Connectors	Samtec	$37,500	50 * 600 + 25% spare		
1.2.6.3.2	Procure TPC FEE LV power supplies					$62,100	
		10AWG 6T00UP Cable	Belden	$6,000	$1.5/ft, 4000ft.		
		MegaPac chassis (5V)	Vicor West Coast	$56,100	5100 * 10 + 1 spare		
1.2.6.3.3	Fabricate and assemble all TPC Fee boards					$117,500	
		Initial fee		$5,000			
		Board fabrication		$75,000	100 * 600 + 25% spare		
		Parts mounting		$37,500	50 * 600 + 25% spare		

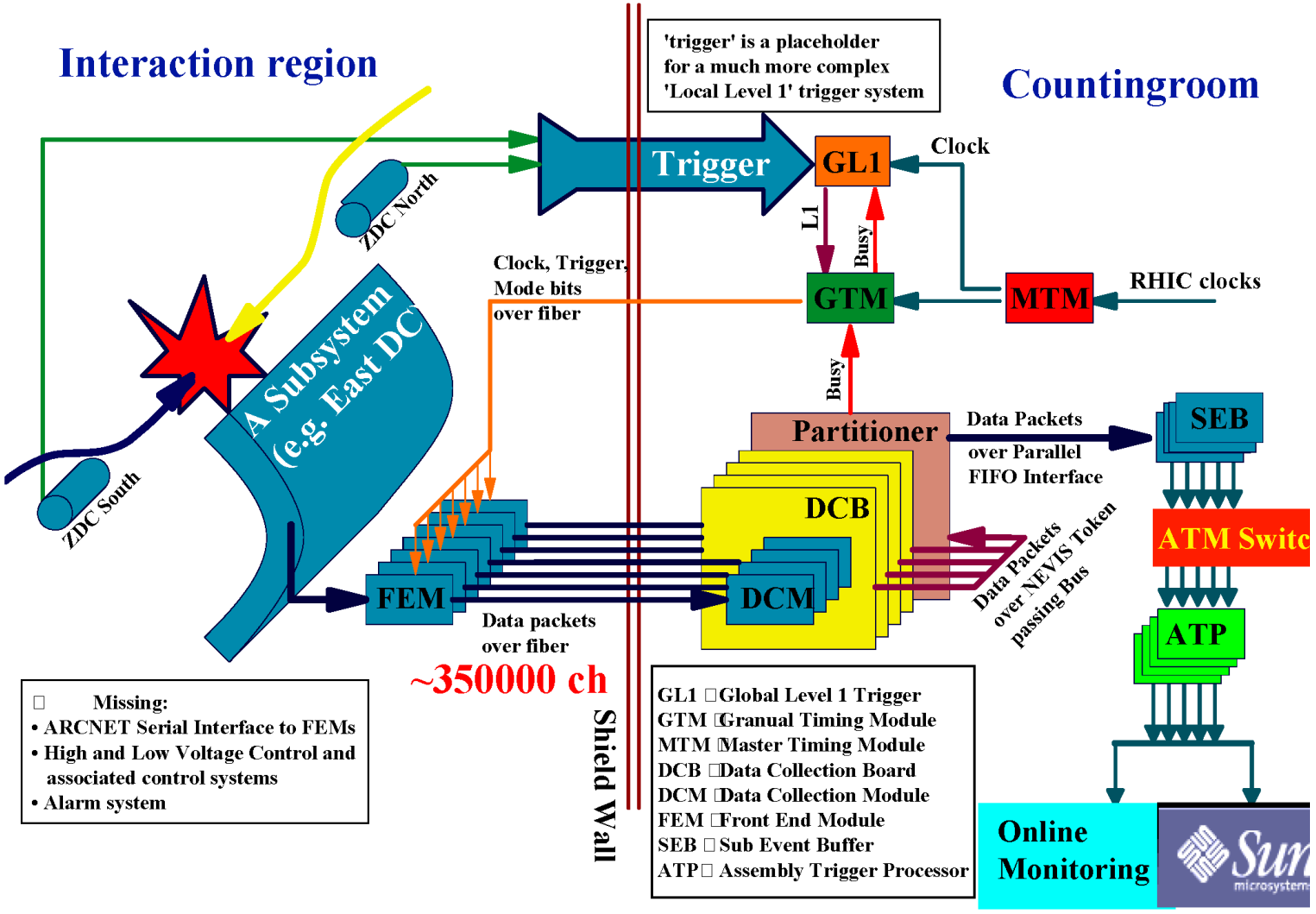
Issue on FEE development

- Common mode noise issue (ALICE found)

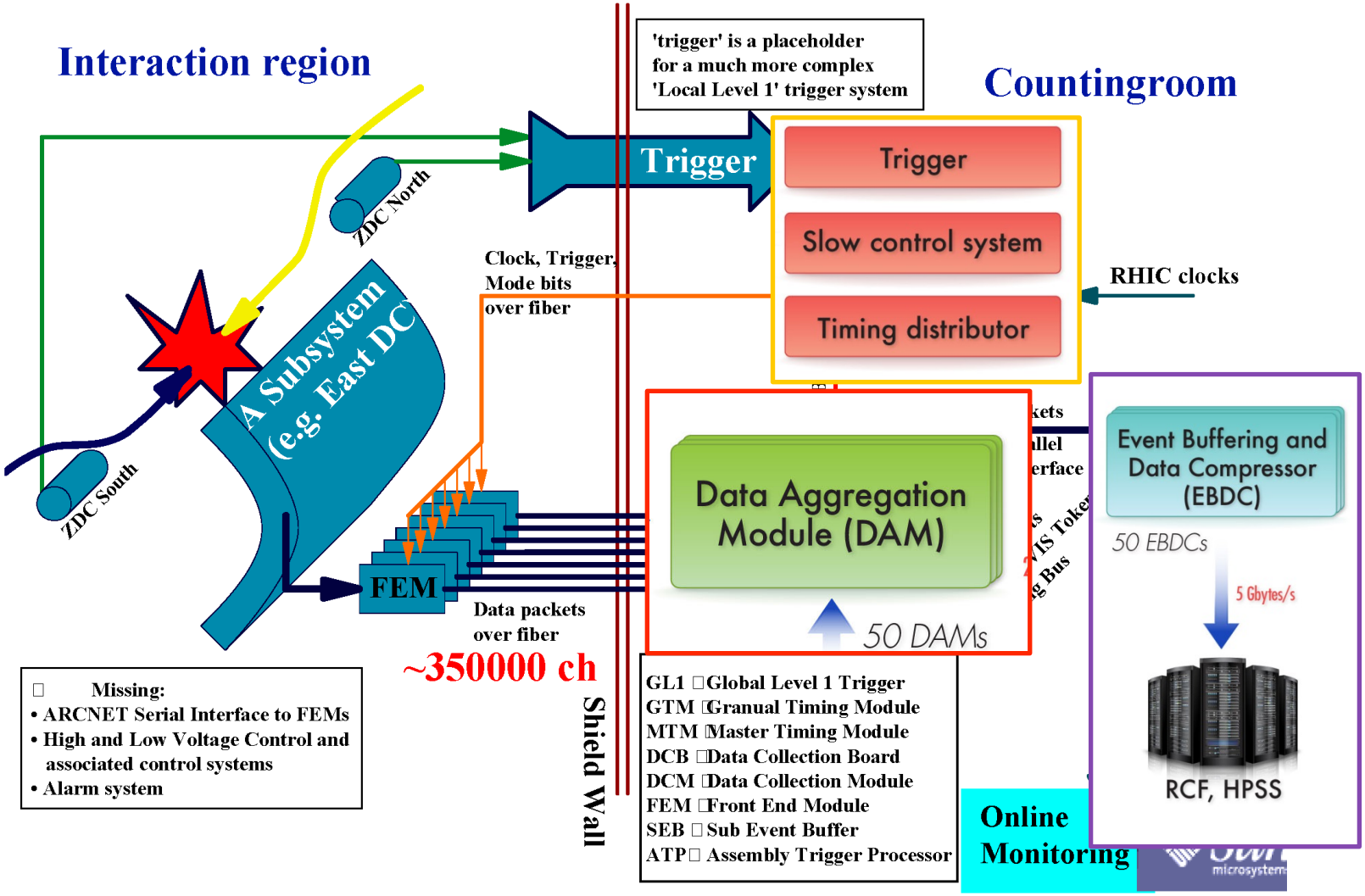


- Common Mode removal is what the on-board DSP for the SAMPA chip is designed to do.
  - But, this is within a chip, i.e. 32 ch
- The technique:
  - Find a large number of “empty channels”.
  - See if they all dip below zero together.
  - Correct everyone up by the amount of the dip.
- ALICE ended up with 5MHZ sampling instead of 10MHz in order to fit the bandwidth of GBTx
  - SAMPA itself can drain all the data

DAQ scheme: PHENIX VS sPHENIX TPC



DAQ scheme: PHENIX VS sPHENIX TPC



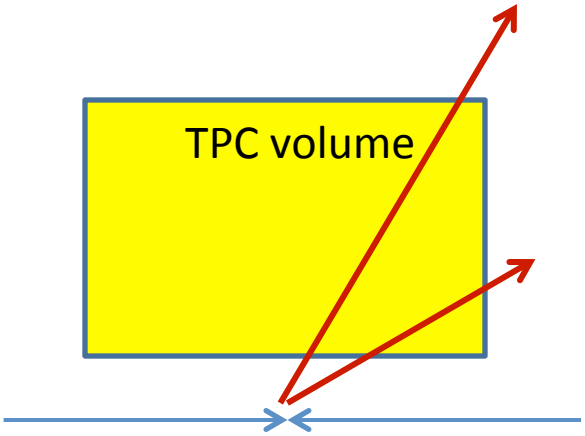
Data rate calculation

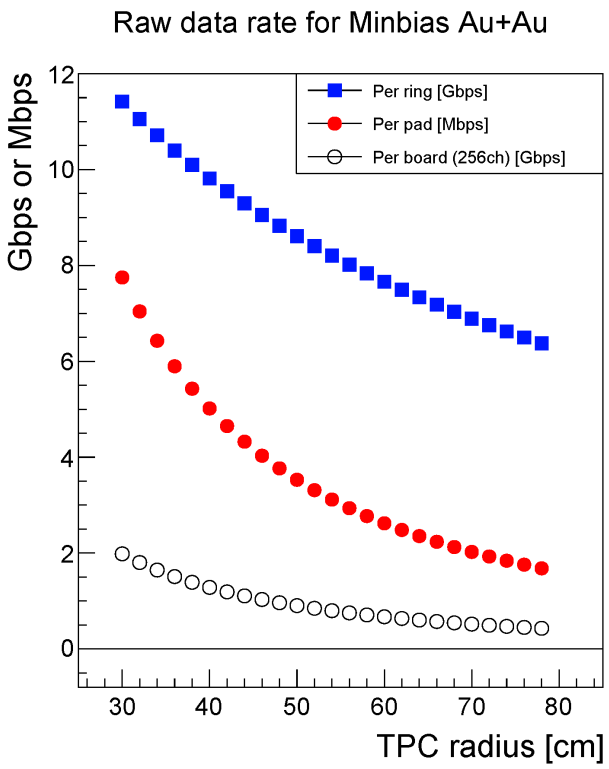
- Raw data (100% duty factor is assumed)
  - Sampling rate in z-direction: 10MHz (= 100nsec)
  - Pulse peaking time is 160nsec (fixed from SAMPA's specification), which leads to ~350nsec for whole pulse shape.
    - More than 4 samples in timing (z) direction is necessary. We decided on taking 5 samples including pre-signal
  - One cluster will be spread over 3 pads in r-ϕ plane
    - Coming from the characteristics of the Ne2K (Ne - CF_4 - iC_4H_{10}: 95% - 3% - 2%) gas
  - We measure 40 clusters for one track
  - Each sample is 10 bits: 40 clusters * 15 * 10 bits = 6 Kbits/track
  - 800 tracks per event: 6Kbits/track * 800 = 4.8 Mbits/event
    - This number doesn't take eta-dependent acceptance change of TPC into account
  - At 100 KHz: 4.8 Mbits/event * 100 KHz = 480 Gbits/s
- With header of SAMPA (40% increase at maximum): 670Gbits/s
  - With eta-dependent acceptance change: 940Gbits/s

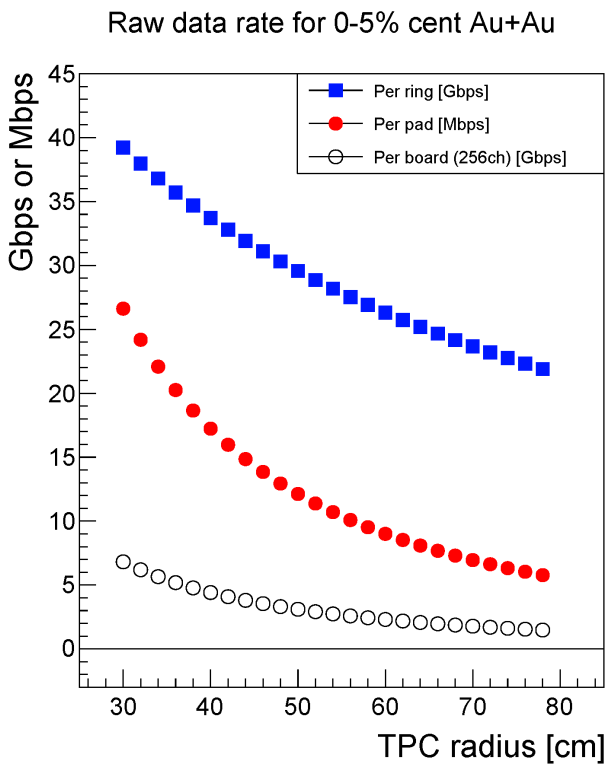
A bit more differential rates

- Radius dependent occupancy and η coverage change are taken into account
- 2 Gbps/board for Minbias, 7 Gbps/board for 0-5% cent Au+Au, @ R= 30cm
  - One board = 256 channels = one optical fiber from FEE to DAM
  - C.f. GBT rate: 4.8 Gbps (line rate), 3.2 Gbps (payload rate)

Per ring: Data rate at [r_1, r_1+1cm]







On recording data at 5GB/sec

From Chris Pinkenburg

- 20 week run (12,096,000 sec)
- 5GB/sec → 60.5 PB
- 75% duty factor → 40PB
- 40PB is only a factor of 4 more than STAR took in 2014 using LTO5 tapes/tape drives, should not be a problem in 2022.
- Current LTO7 (released Dec 2015) store 4x data of LTO5 @ 2x write speed